

What is claimed is:

1 1. A method for testing a semiconductor memory device,  
2 comprising:

3 a first step of generating n number of internal addresses  
4 including an external address supplied for designating a storage  
5 region of data for 1 bit to be written into a storage unit of  
6 a semiconductor memory device, in synchronization with a  
7 high-speed clock which has a frequency n times that of an external  
8 clock (n is a natural number) and is synchronized with the external  
9 clock, generating n bits of internal write data corresponding  
10 to n number of the internal addresses in synchronization with  
11 the high-speed clock and writing the generated internal write  
12 data into the storage unit; and

13 a second step of latching an external address supplied  
14 for designating a storage region of data for 1 bit to be read  
15 from the storage unit, generating n number of internal addresses  
16 including the external address in synchronization with the  
17 high-speed clock, reading n bits of internal read data  
18 corresponding to n number of the internal addresses from the  
19 storage unit in synchronization with the high-speed clock and  
20 outputting the internal read data corresponding to the internal  
21 address, which coincides with the latched external address, out  
22 of n number of the internal addresses.

1 2. The method for testing a semiconductor memory device,  
2 according to claim 1, wherein

3 in the second step, 1 bit of the internal read data read  
4 from the storage unit in accordance with one of n number of the

5 internal addresses, which coincides with the latched external  
6 address and is synchronized with the high-speed clock, is  
7 outputted.

1 3. The method for testing a semiconductor memory device,  
2 according to claim 1, wherein

3 n number of the internal addresses are generated by use  
4 of any one of a first address generating method of generating  
5 the internal addresses by sequentially increasing an address  
6 of the external address, a second address generating method of  
7 generating the internal addresses by sequentially decreasing  
8 the address of the external address and a third address generating  
9 method of generating the internal addresses within a range which  
10 includes the external address and is separated by n.

1 4. The method for testing a semiconductor memory device,  
2 according to claim 1, wherein

3 n bits of the internal write data are generated by use  
4 of any one of a first data generating method of consecutively  
5 generating n number of values of "1", a second data generating  
6 method of consecutively generating n number of values of "0",  
7 a third data generating method of alternately repeating the  
8 values "1" and "0" in this order and a fourth data generating  
9 method of alternately repeating the values "0" and "1" in this  
10 order.

1 5. A test circuit for a semiconductor memory device, comprising:

2 a high-speed clock generating circuit which generates a

3 high-speed clock which has a frequency  $n$  times that of an external  
4 clock ( $n$  is a natural number) and is synchronized with the external  
5 clock;

6 a high-speed address generating circuit which generates,  
7 in synchronization with the high-speed clock,  $n$  number of first  
8 internal addresses including a first external address supplied  
9 for designating a storage region of data for 1 bit to be written  
10 into a storage unit of a semiconductor memory device, latches  
11 a second external address supplied for designating a storage  
12 region of data for 1 bit to be read from the storage unit, outputs  
13 the second external address as a latch address and generates  
14  $n$  number of second internal addresses including the second  
15 external address in synchronization with the high-speed clock;  
16 and

17 a high-speed data generating circuit which generates  $n$   
18 bits of internal write data corresponding to  $n$  number of the  
19 first internal addresses in synchronization with the high-speed  
20 clock, supplies the internal write data to the storage unit and  
21 outputs internal read data corresponding to one of  $n$  number of  
22 the second internal addresses, which coincides with the latch  
23 address, out of  $n$  bits of the internal read data read from the  
24 storage unit in synchronization with the high-speed clock.

1 6. The test circuit for a semiconductor memory device, according  
2 to claim 5, wherein the high-speed data generating circuit  
3 outputs 1 bit of the internal read data read from the storage  
4 unit in accordance with one of  $n$  number of the internal addresses,  
5 which coincides with the latch address and is synchronized with

6 the high-speed clock.

1 7. The test circuit for a semiconductor memory device, according  
2 to claim 5, wherein the high-speed address generating circuit  
3 includes any one of first address generating means for generating  
4 the internal addresses by sequentially increasing an address  
5 of the external address, second address generating means for  
6 generating the internal addresses by sequentially decreasing  
7 the address of the external address and third address generating  
8 means for generating the internal addresses within a range which  
9 includes the external address and is separated by n

1 8. The test circuit for a semiconductor memory device, according  
2 to claim 5, wherein the high-speed data generating circuit  
3 generates n bits of the internal write data by use of any one  
4 of a first data generating method of consecutively generating  
5 n number of values of "1", a second data generating method of  
6 consecutively generating n number of values of "0", a third data  
7 generating method of alternately repeating the values "1" and  
8 "0" in this order and a fourth data generating method of  
9 alternately repeating the values "0" and "1" in this order.

1 9. The test circuit for a semiconductor memory device, according  
2 to claim 5, wherein

3 the high-speed address generating circuit includes an  
4 external address fetch/latch circuit and an internal address  
5 generating circuit,

6 the external address fetch/latch circuit fetches the

7 external address, latches the external address to be supplied  
8 to the high-speed data generating circuit as a latch address  
9 and transfers the fetched external address to the internal  
10 address generating circuit, and  
11 the internal address generating circuit generates, in  
12 synchronization with the high-speed clock, n number of the  
13 internal addresses including the external address supplied from  
14 the external address fetch/latch circuit.